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EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,450	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24-26,28-30 and 32-35* is/are pending in the application.

4a) Of the above claim(s) *1-19* is/are withdrawn from consideration.

5)☒ Claim(s) *22,24 and 25* is/are allowed.

6)☒ Claim(s) *20,21,26,28-30,32 and 33* is/are rejected.

7)☒ Claim(s) *34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 20, 2003 has been entered.

Claim Renumbering

2. Claim 31, which was canceled by the Applicant in the response filed on August 15, 2002, paper No. 9, has been renumbered as claim 35. "C.F.R. § 1.126

Claim Objections

3. Claim 20 is objected to because of the following informalities: In part (c) of the claim, the word "spattering" should be replaced with "sputtering". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20, 21, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,837,578 to Fan et al. in view of US patent No. 6,316,802 to Schindler et al.

Regarding claim 20, Fan et al. teaches a method of manufacturing an integrated circuit, comprising the steps of:

forming a C.O.B. structure (Col. 3, lines 20-23), which would have inherently required forming bit lines and contacts in a first insulating film;

forming a second interlayer insulating film (33) and electrode-forming insulating film (36);

etching holes in the electrode-forming insulating film (Fig. 3(e));

forming a conductive film (39) in the holes, and removing the electrode-forming insulating film to form cylindrical capacitor first electrodes (Fig. 3(h));

depositing a ferroelectric capacitor dielectric film (310) over the first electrodes; and

depositing and patterning a first a conductor layer (311) to form a second electrode.

Fan et al. does not teach forming a metal or metal compound for forming the lower electrode. Fan et al. does not teach patterning first and second conductor layers to form second electrodes, wherein the second conductor layer is ruthenium formed by sputtering. Fan et al. does not teach depositing a third interlayer insulating film to cover the second electrodes, and forming connection holes reaching the second electrodes and the first layer wiring.

Schindler et al. teaches using a metal to form the lower electrode (21) of a ferroelectric capacitor, patterning first (23a) and second (23b) conductor layers to form second electrodes and forming a third insulating film (25) and forming a connection hole to the second electrode and first wiring layer.

Schindler teaches a layered upper electrode comprising a noble metal for the lower layer (23a) and a conductor for the upper layer (23b). If an oxide forms on the electrode layer, it would result in a low-k dielectric forming between the ferroelectric layer and the electrode and a reduction of capacitance. Schindler et al. does not teach using ruthenium formed by sputtering to form the conductor layer. Ruthenium, being a noble metal, is resistant to oxidation when subjected to the high temperatures that are necessary for processing high-k films. Ruthenium also has a high melting point. Additionally, Ruthenium is an art-recognized substitute for platinum, and since it is also a noble metal and would be expected to have similar properties to platinum. It would have been obvious to one of ordinary skill in the art to use ruthenium since it is a known material that is well suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

It is also desirable to form a connection to the capacitor to give it functionality in the integrated circuit. Since etching is a well known method of forming contact holes in insulation film, it would have been obvious design choice to employ this known method of forming contacts. Schindler et al. further teaches contact holes to the second

electrode and the wiring layer. It would have been obvious to incorporate the teaching of the first and second contact holes since it is desirable to enable communication between the capacitor and active devices.

Sputtering is a well-known method of depositing metal layers. It would have been obvious to one of ordinary skill in the art to use a known method as opposed to

Regarding claim 21, Fan et al. does not teach using the second layer of the second electrode as a mask to form the first layer of the second electrode after the second layer is etched. Schindler et al. teaches a method wherein the second electrode is formed in layers. Since the tungsten layer is formed directly on top of the first conductive layer, it would have to be etched before etching the first conductive layer layer. It would have been obvious to incorporate the teaching of Schindler et al. into the method taught by Fan et al. for reasons discussed above.

Regarding claim 26, Fan et al. teaches a method of making an integrated circuit, comprising the steps of:

forming first electrodes on a first insulating film;

forming a capacitor dielectric film over the first electrode; and

forming continuous second electrodes over the capacitor dielectric film.

Fan et al. does not teach a method wherein the formation of the second electrode includes forming a first metal layer. Fan et al. does not teach a second metal layer having a greater thickness and lower resistivity than the first metal layer. Fan et al. does not teach forming a second insulating film over the second electrodes, wherein the film has an opening for exposing a part of the second electrodes, wherein a

photoresist film is used as a mask and a conductive layer is formed inside the opening. Schindler et al teaches a method, wherein the second electrode comprises a first and second metal layer, the second metal layer have a greater thickness and lower resistivity than the first metal layer (Col. 4, lines 43-44; Col. 1, lines 58-60; Col. 3, lines 5-7). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schindler et al. into the teaching of Fan et al. for reasons discussed above.

Schindler et al. further teaches forming a second insulating film (25) with an opening having a conductor layer (26) inside. Schindler et al. is silent with respect to the method used to form the contact hole. One having ordinary skill in the art would have been required to select a known method of forming the opening. The use of photoresist to form patterns is well known in the art, as well as ashing the resist to remove it. Therefore, It would have been obvious to use a photoresist mask and ashing to form the contact hole. It would have been obvious to include the process of forming the contact hole into the method taught by Fan et al. since it is desirable to provide connection to other circuitry, such as bit lines and drive lines.

Neither Fan et al. nor Schindler et al. teach using ruthenium for the first layer of the multi-layered electrode. Ruthenium is an art-recognized substitute for platinum, as well as being a known material that is well suited for the intended use, as discussed above with respect to claim 21. It would have been obvious to one of ordinary skill in the art to use ruthenium for the same reasons as those discussed in the rejection of claim 21.

Regarding claim 28, Fan et al. does not teach a method of producing a semiconductor device, wherein the first metal layer is platinum or ruthenium and the second metal layer is tungsten or tungsten nitride. Schindler et al teaches a method, wherein the first metal layer is platinum and the second metal layer is tungsten. It would have been obvious to one of ordinary skill to incorporate the teaching of Schindler et al. into the method taught by Fan et al. for reasons discussed above.

6. Claims 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of US patent No. 5,854,104 to Onishi et al.

Regarding claim 22, Fan et al. teaches a method of making an integrated circuit, comprising the steps of:

forming first electrodes on a first insulating film;

forming a capacitor dielectric film over the first electrode; and

forming second electrodes over the capacitor dielectric film.

Fan et al. does not teach forming a second insulating film over the second electrodes, wherein the film has an opening for exposing a part of the second electrodes, wherein a photoresist film is used as a mask and a conductive layer is formed inside the opening. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a first metal layer by CVD. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over the first metal layer.

Onishi et al. teaches forming a second insulating film (18) over the second electrode having an opening for exposing a part of the second electrodes (Col. 7, lines

38 – 43). The opening would have inherently included a conductive layer, since the purpose of the opening is to provide electrical contact to a circuit. Onishi et al. teaches a method wherein forming the second electrode includes depositing a platinum layer by a known method (Col. 5, lines 12 and 13). Onishi et al. teaches a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over and directly contacting the first metal layer. It would have been obvious to one of ordinary skill in the art to form the opening in the second insulating film since it is desirable to form a connection to the capacitor to give it functionality in the integrated circuit. It would have further been obvious to provide a conductor layer in the opening since it is needed to provide a connection. It would have been obvious to use CVD to deposit the metal since it is a known method, as suggested by Onishi et al. It would have been further obvious to incorporate the method taught by Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Onishi et al. does not disclose using a photoresist mask to form the contact hole and the ashing the photoresist. Onishi et al. is silent with respect to how the contact hole. One having ordinary skill in the art would have been required to select a known method of forming the opening. The use of photoresist to form patterns is well known in the art, as well as ashing the resist to remove it. Therefore, It would have been obvious to use a photoresist mask and ashing to form the contact hole.

Neither Fan et al. nor Onishi et al. teach using ruthenium for the first layer of the multi-layered electrode. Ruthenium is an art-recognized substitute for platinum, as well as being a known material that is well suited for the intended use, as discussed above

with respect to claim 21. It would have been obvious to one of ordinary skill in the art to use ruthenium for the same reasons as those discussed in the rejection of claim 21.

Regarding claims 24 and 33, Fan et al. does not teach a method, wherein the second metal layer comprises tungsten or tungsten nitride. Onishi et al. teaches a method, wherein the second metal layer comprises titanium nitride. It would have been obvious to one of ordinary skill in the art to substitute titanium nitride with tungsten nitride since the two refractory metals have similar properties.

Regarding claims 25 and 30, Fan et al. does not teach a method of making an integrated circuit, wherein the second metal layer is formed by sputtering. Onishi et al. teaches a method of making an integrated circuit, wherein the second metal layer is formed by sputtering (Col. 5, lines 9-14). It would have been obvious to incorporate the teaching of Onishi et al. into the teaching of Fan et al. for reasons discussed above.

Regarding claim 29, Fan et al. teaches a method of making an integrated circuit, including the steps of:

forming a first electrode over a first insulating film;

forming a capacitor dielectric over the first electrode; and

forming a second electrode over the capacitor dielectric.

Fan et al. does not teach a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer. Onishi et al. teaches a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer, wherein the second metal layer has a higher oxidation resistance than

ruthenium. It would have been obvious incorporate the teaching of Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Onishi et al. does not teach using a ruthenium film for the first metal layer. Onishi et al. teaches using platinum for the first metal layer. It would have been obvious to one having ordinary skill in the art to use ruthenium in place of platinum since it is also a noble metal with a high-melting point and it is well suited for the intended use.

Allowable Subject Matter

7. Claims 22, 24 and 25 are allowed.

8. Claims 34 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach a method, wherein forming the second electrodes includes the steps of forming a first ruthenium film *containing oxygen* and a metal layer *not containing oxygen*.

Response to Arguments

10. Applicant's arguments filed May 20, 2003 have been fully considered but they are not persuasive.

11. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Applicant argues that Schindler et al. does not teach that the second film (23b) has sufficient oxidation resistance and therefore does not recognize the advantages of depositing the first metal layer using CVD, and the second layer by sputtering. Schindler et al. teaches forming that the second metal layer can be done by a standard method, giving CVD *as an example* (Col. 4, lines 48 – 51). Schindler et al. further teaches that the platinum layer can be applied using sputtering, as *an example*. Although Schindler et al. gives sputtering as an example of a method to form the first metal layer, and CVD as an example of a method to form the second metal layer, they are both understood to be standard methods of depositing the metal layers. It would be obvious to one of ordinary skill to select either method, even though The Applicant may have found certain advantages of using one over the other. The methods of deposition are the most widely used in semiconductor processing.

The Applicant argues that the prior art does not incorporate the use of ruthenium into the electrodes. The Applicant further argues that the prior art does not teach using a photoresist as a mask to form openings in a third insulation film and then ashing the photoresist and forming a conductor in the opening. These arguments are addressed above in the rejection of the claims.

The Applicant further asserts that the limitation of the metal layer having higher resistance to oxidation than ruthenium. Schindler et al. teaches this feature, as discussed above in the rejection of the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DWO
June 16, 2003